Amendments to Specification:

Please replace the paragraph beginning at page 1, Line 6 with the following paragraph:

This application claims priority of U.S. Provisional Patent Application Number 60/414,725 (Attorney Docket No. KLA1P067P/P995P), filed 27 September 2002, which application is incorporated herein by reference in its entirety for all purposes. This application is filed concurrently with and related to the following patent application: United States Nonprovisional Application Number: 10/673,058 (Attorney Docket No. KLA1P068), entitled "METHOD AND APPARATUS USING MICROSCOPIC AND INTERFEROMETRIC BASED DETECTION" naming Hwang et al. as inventors. The above-referenced US Patent Application is incorporated herein by reference in its entirety for all purposes.

Please replace the paragraph beginning at page 2, Line 4 with the following paragraph:

Conventional optical metrology techniques use intensity based or scattering based systems. With intensity based systems it is difficult to detect dark defects sitting in dark structures or to differentiate from other defects with similar contrast. High Aspect ~~Ration~~ ratio Inspection (HARI) refers to the inspection of High Aspect Ratio (HAR) structures. HARI provides difficult wafer inspection challenges to chipmakers, especially as the integrated circuits become smaller. Because the background is darker, slight perturbations may not easily be discriminated against the background. Furthermore, dark structures provide relatively low signal levels.

Please replace the paragraph beginning at page 8, Line 7 with the following paragraph:

Figure ~~2A~~ 2 is a flowchart illustrating a conceptual flow of an integrated circuit design process and an inspection process used to identify defects in the fabricated dies in accordance with one embodiment of the present invention.

Please replace the paragraph beginning at page 13, Line 16 with the following paragraph:

Preferably, the illumination provided shall have sufficient temporal coherence such that the fringe contrast is adequate even if there is an optical path difference between the path to the wafer and the path to the reference mirror. In one embodiment, compensation for insufficient temporal coherence of the illumination source includes removal of the reference module and the addition of a tilted reference mirror to location A (in FIG. 3A), which is the conjugate plane to the wafer, so the optical path length between the reference arm and the test arm is equal. According ~~ot~~ to various embodiments, the illumination is either continuous or pulsed depending on the image acquisition scheme.

Please replace the paragraph beginning at page 16, Line 6 with the following paragraph:

Figure ~~2A~~ 2 is a flowchart illustrating a conceptual flow of an integrated circuit design process 200 and an inspection process used to identify defects in the fabricated dies in accordance with one embodiment of the present invention. Initially, in operation 202, an integrated circuit (IC) device is designed using any suitable design techniques. For example, an IC designer may use preexisting schematic library blocks to form the IC device using, for example, electronic design automation (EDA) tools. In some cases, the IC designer may create the IC device or part of the IC device from scratch with the aid of any suitable design system, such as conventional computer aided design (CAD) tools. For example, the IC designer may use a schematic CAD tool to plan the logic diagrams for a particular IC device. Still further, the IC designer may write a description of the IC device or portions of the IC device with the aid of a hardware design language, such as VHDL.

Please replace the paragraph beginning at page 28, Line 3 with the following paragraph:

In a further example, the inspection ~~subsytem~~ subsystem 360 may be arranged to include an illumination beam 308 generated from a coherent illumination source, and the beam splitter 305 having a special coating designed to reflect a spectral band from the coherent source along the optical path towards the wafer 346 and to permit all other spectral bands in the illumination beam 308 to pass through to the reference module 314. A dichroic surface 316 is placed in this second optical path to serve as a reference mirror for implementing a first operational mode of topographic metrology as described U.S. Patent No. 4,818,110, which is incorporated by reference herein. However, in one embodiment of the present invention, a complex field inspection may be performed in a second operational mode by selecting the illumination source such that, the reference beam passes through the dichroic surface 316 without reflection.

Please replace the paragraph beginning at page 34, Line 10 with the following paragraph:

Once depolarization occurs, the complex field information for that portion cannot be determined. That is, depolarization ~~leadsto~~ leads to the reduction in fringe visibility. But, the complex field information, generally designed to discern subtle deflects, is unnecessary in the presence of such information indicating a large defect. If fringe modulation is noted, the processing block identifies the areas as containing a defect. The matching of measured fringe modulations to known fringe modulation patterns may take place in post-data processing block 340 (See FIG. 3A), similar to the pattern matching performed with phase difference measurements as described further above with respect to FIG. 3A. Processing as to the portions of the wafer showing no defects continues.